REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-11, 19-28, 38-43, 50-63, and 65-69 are presently active in this case, Claims 12-18, 29-37, 44-49, 64, and 70-76 having been canceled without prejudice or disclaimer and Claim 69 having been amended by way of the present Amendment. The Applicant respectfully requests entry of the amendments set forth herein as they merely cancel claims and place the application into condition for allowance.

Claims 19-28, 38-43, 50-63, 65, and 68 are allowed, and Claims 3-11 have been indicated as being allowable if rewritten in independent form.

The non-elected claims have been canceled without prejudice or disclaimer.

In the outstanding Official Action, Claims 1, 2, 64, 66, 67, 69, and 76 were rejected under 35 U.S.C. 102(a) as being anticipated by Saruta et al. (EP 1 004 450 A2). For the reasons discussed below, the Applicant traverses the anticipatory rejection.

In the Office Action, the Saruta et al. reference is indicated as anticipating each of independent Claims 1, 66, and 67. However, the Applicant notes that a claim is anticipated only if each and every element as set forth in the claims is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). As will be demonstrated below, the Saruta et al. reference clearly does not meet each and every limitation of the independent Claims 1, 66, and 67.

Claim 1 recites a printing material container comprising, among other features, a

storage element having a plurality of non-volatile storage areas that are sequentially accessed, and a storage element control unit that is initialized at a first level of the input reset signal and carries out a writing/reading operation of data into and from the storage element according to the data signal synchronously with the input clock signal when the reset signal is switched over to a second level. Claims 66 and 67 recite methods comprising steps of resetting a count on an address counter to an initial value and prohibiting increment of the count synchronously with a clock signal, in response to detection of a reset signal, setting a direction of data transfer with regard to a data bus, allowing increment of the count on the address counter synchronously with the clock signal after completion of the settings of the directions of data transfer, and reading or writing according to the count on the address counter. The Applicant submits that the Saruta et al. reference does not disclose all of the above features recited in Claims 1, 66, and 67.

The Saruta et al. reference describes a storage element (80) of ink cartridges. The storage unit (80) includes a memory cell (81), a read/write controller (82), and an address counter (83). The read/write controller (82) is a circuit that controls reading and writing operations of data from and into the memory cell (81). The controller (46) of the print controller (40) is configured to make a chip select signal (CS), which sets the storage element (80) in an enabling state, in a high level at step ST21. While the chip select signal (CS) is kept at the low level, the count on the address counter (83) is set equal to zero. When the chip select signal (CS) is set to the high level, the address counter (83) is enabled to start the count. The controller (46) then generates a required number of pulses of the clock signal (CLK) to specify an address, at which data are written, at step ST22. The address decoder

(95) incorporated in the print controller (40) is used to determine the required number of pulses of the clock signal (CLK). The address counter (83) included in the storage element (80) counts up in response to the required number of pulses of the clock signal (CLK) thus generated. During this process, a read/write signal (R/W) is kept in a low level. This means that an instruction of reading data is given to the memory cell (81). Dummy data are accordingly read synchronously with the output clock signal (CLK).

After the address counter (83) counts up to the specified address for writing data, the controller (46) carries out an actual writing operation at step ST23. The writing operation switches the read/write signal (R/W) to the high level, outputs one-bit data to a data terminal I/O, and changes the clock signal (CLK) to a high active state on the completion of data output. While the read/write signal (R/W) is in the high level, data (DATA) of the data terminal I/O are written into the memory cell (81) of the storage element (80) synchronously with a rise of the clock signal (CLK). Although the writing operation starts synchronously with a fifth pulse of the clock signal (CLK) in the example of FIG. 7B, this only describes the general writing procedure. The writing operation of required data, for example, the remaining quantity of ink, may be carried out at any pulse, for example, at a first pulse, of the clock signal (CLK) according to the requirements.

The Applicant submits that the Saruta reference does not disclose a storage element control unit that is initialized at a first level of the input reset signal and carries out a writing/reading operation of data into and from the storage element according to the data signal synchronously with the input clock signal when the reset signal is switched over to a second level. The printing material container recited in Claim 1 of the present application

uses the switchover of the reset signal between the high level and the low level so as to carry out a writing/reading operation of data. The device of the Saruta reference always needs a combination of the chip select signal and R/W signal to read and write data. This is evident from the fact that a writing operation is not carried out when the R/W signal is at its low level even if the chip select signal is at its high level. Thus, the Saruta reference fails to disclose a storage element control unit that carries out a writing/reading operation of data into and from a storage element according to a data signal synchronously with an input clock signal when a reset signal is switched over to a second level.

Accordingly, the Applicant submits that the Saruta reference fails to disclose all of the limitations recited in Claim 1, and therefore the Saruta reference does not anticipate Claim 1. Furthermore, the printing material container recited in Claim 1 is capable of carrying out an operation, which conventionally requires two signals, with only one signal, and thus the container is not obvious in view of the Saruta reference.

Regarding Claims 66 and 67, the printing material container recited in these claims comprise the steps of "resetting," "setting" and "allowing," which are not disclosed by the Saruta reference. The Saruta reference does not specifically disclose an address count operation. In other words, based on the teachings in the Saruta reference, one of ordinary skill in the art could not attain present Claims 66 and 67, which specify the concrete steps of an address count operation, by referring to the Saruta reference that provides no explicit disclosure of an address count operation.

Claims 66 and 67 recite resetting a count on an address counter to an initial value and prohibiting increment of the count synchronously with a clock signal, in response to detection

of a reset signal, setting a direction of data transfer with regard to a data bus and a direction of data transfer with regard to the storage element, and allowing increment of the count on the address counter synchronously with the clock signal after completion of the settings of the directions of data transfer. The Saruta reference does not disclose allowing the increment on the count of the address counter to occur simultaneously with the clock signal after completion of the settings of the directions of data transfer. The Saruta reference discusses allowing the address counter (83) to start the count when the chip select signal (CS) is set to the high level. Other than this discussion, the Saruta reference does not provide detailed disclosure of the address count operation, and clearly does not disclose all of the limitations explicitly recited in Claims 66 and 67 of the present application.

Accordingly, the Applicant respectfully requests the withdrawal of the anticipation rejection of Claims 1, 66, and 67.

The rejected dependent claims are considered allowable for the reasons advanced for the independent claim from which they depend.

Consequently, in view of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance and an early and favorable reconsideration of this application is therefore requested.

Respectfully Submitted,

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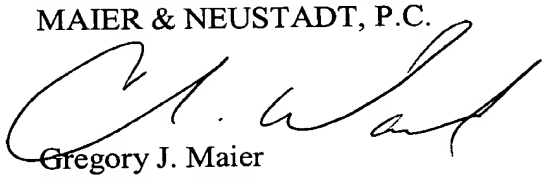

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